Analytical Compact Modeling of Nanoscale Triple-Gate FinFETs


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Abstract—An analytical compact drain current model for undoped (or lightly doped) short-channel triple-gate (TG) FinFETs is presented, taking into account quantum mechanical and short-channel effects such as threshold voltage shift, drain-induced barrier lowering and subthreshold slope degradation. In the saturation region, the effects of series resistance, surface-roughness scattering, channel-length modulation and saturation velocity were also considered. The proposed model has been validated by comparing the transfer and output characteristics with device simulations for channel lengths down to 20 nm.

I. INTRODUCTION

Triple-gate (TG) field-effect transistors such as FinFETs have been recognized as the best candidates for sub-100 nm scaling of MOSFETs due to their immunity to short channel effects (SCEs) and proximity to standard bulk planar CMOS processing [1]. To our knowledge, the work published so far on drain current modeling in TG FinFETs is very limited [2], [3]. In [2], to calculate the threshold voltage the inversion potential $\phi_i$ was determined as a fitting parameter independent of the channel geometry. However, it is not clarified if this value of $\phi_i$ is valid for any gate oxide thickness, whereas the model was verified only in transfer characteristics. More recently, in [3] an analytical drain current model has been proposed in IFET transistors, however, this model is limited in the linear region of operation and was validated only in transfer characteristics for channel length down to 40 nm.

In this work, based on analytical models for the threshold voltage and subthreshold slope developed for undoped or lightly doped DG and TG MOSFETs [4] and relying on our previous analytical modeling of drain current in DG MOSFETs [5], we derive a fully analytical and compact drain current model valid in all regions of operation for TG FinFETs, including SCEs, CLM, QMEs and other secondary effects, such as mobility degradation and series resistance. The unique features of the present model are the use of unified expressions for the inversion charge and drain current valid in all the regions of operation. The proposed compact model has been validated down to channel length equal to 20 nm using the device simulator Silvaco (Atlas).

II. COMPACT DRAIN CURRENT MODEL

A schematic view of the TG FinFET is shown in Fig. 1, where $W_{fin}$ is the fin width, $H_{fin}$ is the fin height and $L$ is the channel length. The gate electrode surrounds the silicon body on three sides with a gate oxide thickness $t_{ox}$. The body of the silicon is lightly doped with acceptor concentration $N_A$ and the gate material is metal with proper work function to adjust the threshold voltage.

A. Compact Drain Current Equation

In undoped or lightly doped short-channel DG FinFETs, the total drain current can be expressed as a synthesis of the currents in subthreshold and strong inversion regimes, using a suitable interpolation function [5]. Both subthreshold and strong inversion currents can be expressed in terms of the normalized sheet charge density, where $q$ is the electronic charge, $\varepsilon_{Si}$ is the permittivity of silicon and $kT$ is the thermal energy. In strong inversion, the normalized sheet charge density in short-channel DG FinFETs is given by [5]

$$ q_{th} = \frac{W_{fin}}{e_{ox} L} \text{LambertW} \left( \frac{q k T}{e} \right) \left( \frac{V_{th} - \Delta \phi}{k T \ln(N_A/n_i)} \right) $$

(1)

where $e_{ox}$ is the permittivity of the gate oxide, $V_s$ is the electron quasi-Fermi potential which varies from the source voltage 0 to the drain voltage $V_d$, $Vb=\Delta \phi-(kT/q)\ln(N_A/n_i)$ is the flat-band voltage, $\Delta \phi$ is the gate work function referenced to silicon, $N_A$ is the doping concentration of silicon, $n_i$ is the intrinsic carrier concentration and $\Delta V_t$ is the threshold voltage roll-off expressed in an analytical form in [5]. Rewriting the above equation in the form of

$$ q_{th} = \frac{W_{fin}}{e_{ox} L} \text{LambertW} \left( \frac{e}{2kT} \left( V_s + \Delta \phi - V_b - V_d \right) \right) $$

(2)

and equating (2) with (3)

$$ q_{th} = \frac{W_{fin}}{e_{ox} L} \text{LambertW} \left[ \frac{e}{2kT} \left( V_s + \Delta \phi - V_b - V_d \right) \right] $$

(3)

we derive the threshold voltage $V_t'$ for DG FinFETs

$$ V_t' = V_b - \frac{A_{1, DG}(V_{th} + V_d) + A_{2, DG}V_{th} - \phi_i \ln \left( \frac{Q_{th} N_A}{n_i e_{ox} W_{fin}} \right)}{1 - \left( A_{1, DG} + A_{2, DG} \right)} $$

(4)

where $\phi_i = kT/q$ and $A_{1, DG}$ and $A_{2, DG}$ are parameters expressed as a function of the device natural length and channel length [3], whereas the minimum carrier sheet density $Q_{th}$ adequate to achieve the turn-on condition, is given by the analytical expression.
The DG FinFET $V'_1$ model can be extended to the TG FinFET $V'_1$ model using effective parameters capturing the electrostatic control of the top gate over the SCEs given by [3]:

$$V'_e = V'_b - \frac{A_{1,TG}(V'_s + V'_d) + A_{2,TG}V'_s - \phi \ln \left( \frac{Q/N}{\kappa^2 W_{fin}} \right)}{1 - (A_{1,TG} + A_{2,TG})}.$$  

(6)

The parameters $A_{1,TG}$ and $A_{2,TG}$ are geometrical factors expressed as a function of $\lambda_{sym}$ and $\lambda_{asym}$ representing the natural lengths of the symmetric and asymmetric DG MOSFETs composing the TG FinFETs [3]. These two characteristic lengths are associated with the conductive path of the “virtual cathode” in the silicon channel, expressed as:

$$\lambda_{sym} = \frac{1}{2} \left( \frac{W_{fin}}{e_{fin}} + \frac{3W_{fin}}{16} \right)$$

$$\lambda_{asym} = \frac{1}{2} \left( \frac{H_{fin}}{e_{fin}} + \frac{7H_{fin}}{16} \right)$$

(7)

To define the drain current equation in nanoscale TG FinFETs, we start from the unified charge-based equation of short-channel DG MOSFETs valid in all regions of operation, which can be written as [6]:

$$I_d = \mu_n \frac{2W}{L} \left( \frac{2kT}{q} \right) \left( q_{sa} - q_{sd} \right) + \frac{1}{2} \left( q_{sa}^2 - q_{sd}^2 \right),$$

(8)

where $\mu_n$ is the electron mobility and $W$ is the channel width. The first charge term in (8) dominates in the subthreshold region and the second charge term in the above threshold region. $q_{sa}$ and $q_{sd}$ are the values of the normalized inversion charge densities calculated at the source ($V_s = 0$) and drain ($V_s = V_d$), respectively. The unified normalized inversion sheet charge density is described by the relationship [6]:

$$q_{sa} = \text{Lambert}W \left( \frac{q_{sa} - V_s}{\phi} \right) e^{-\frac{q_{sa} - V_s}{2kT}}$$

$$q_{sd} = \text{Lambert}W \left( \frac{q_{sd} - V_d}{\phi} \right) e^{-\frac{q_{sd} - V_d}{2kT}}$$

(9)

where $\phi = 1 \text{ V}$ represents a normalizing factor and $c_1$ is a fitting parameter. The first term of the LambertW function dominates in the subthreshold region, whereas the second term in the above threshold region. The parameter $\eta'$ in Eq. (9) is the subthreshold swing coefficient [3]:

$$\eta' = \frac{1}{1 - 2(A_{1,TG} + A_{2,TG})}$$

(10)

For TG FinFETs, we apply Eq. (8) because for the case of $H_{fin} > W_{fin}$ most of the current will flow along the side-gates. Each half of the top-gate width $W_{fin}$ will contribute to the side-gate of width $H_{fin}$ and, therefore, the effective width of the TG FinFET is $W = H_{fin} + W_{fin}/2$. As a result, the drain current equation in TG FinFETs is similar to this of DG MOSFET with increased channel width. Furthermore, the influence of the top-gate on the SCEs is captured through the threshold voltage defined in (5). In order to improve the computational speed for the current calculation, we use the following approximation for the LambertW(x) function, which has a good accuracy for all positive $x$ [7]:

$$\eta_s = \text{Lambert}W(x) \approx \ln(1 + x) \left( 1 - \frac{\ln[1 + \ln(1 + x)]}{2 + \ln(1 + x)} \right)$$

(11)

### B. Channel Length Modulation

When the drain-source voltage $V_d$ is increased beyond the saturation voltage $V_{d,sat}$, a pinch-off occurs in the channel moving from the drain toward the source. This displacement, known as the channel length modulation effect (CLM), makes the channel shorter than the physical gate length $L$. The so-called electrical gate length $L'$ is then given by $L' = L - \Delta L$ where $\Delta L$ corresponds to the gap between $L$ and the channel pinch-off and is written as [8]:
\[ \Delta L = \lambda_{\text{eff}} \ln \left[ 1 + \frac{V_{\text{def}} - (V_g - V_r)}{V_E} \right]. \]  

(12)

\[ V_E \] is a fitting parameter, \( \lambda_{\text{eff}} \) corresponds to the effective natural length which is the average of the two natural lengths \( \lambda_{\text{sym}} \) and \( \lambda_{\text{asym}} \) given for TG FinFETs by [9]:

\[ \lambda_{\text{eff}} = \sqrt{\left( \frac{1}{\lambda_{\text{sym}}} \right)^2 + \left( \frac{0.5}{\lambda_{\text{asym}}} \right)^2}. \]  

(13)

In (12), \( V_{\text{def}} \) is the effective drain voltage defined as:

\[ V_{\text{def}} = (V_g - V_r) + \left[ (V_d - (V_g - V_r)) + 0.25 \right] \tanh \left( \frac{V_d}{(V_d - (V_g - V_r)) + 0.25} \right)^2. \]  

(14)

Considering the CLM effect, we can write Eq. 8 as:

\[ I_d = 2W \mu_{\text{eff}} \frac{g_{\text{sat}}}{t_{\text{ox}}} \left( \frac{2kT q}{q} \right)^2 q_{\text{sd}} - q_{\text{sd}} + \frac{1}{2} \left( q_{\text{sd}}^2 - q_{\text{sd}} \right) \left( V_d - V_r \right) \]  

(15)

In Eq. (15), the electrical gate length \( L' \) is involved only in the second term in brackets because the first one becomes insignificant when \( V_d > V_{\text{sat}} \).

C. Mobility Degradation and Series Resistance

To include within the effects of series resistance \( R_{\text{sd}} \), saturation velocity \( \nu_{\text{sat}} \) and surface-roughness scattering \( \theta \) we replace in (15) the electron mobility \( \mu_e \) with the function [5]:

\[ \mu_{\text{eff}} = \frac{\mu_e}{1 + \left( 1 + \frac{\mu_e V_d}{\nu_{\text{sat}} (L - \Delta L)} \right) \left( R_{\text{sd}} \frac{W_{\text{eff}} C_{\text{ox}}}{L - \Delta L} \right) (V_g - V_r)}. \]  

(16)

The above mentioned function is modified compared to that in [5] by replacing the series resistance \( R_{\text{sd}} \), with an effective value normalized with respect to the fin width \( R_{\text{sd}} W_{\text{fin}} \), which was found experimentally to be independent of the fin width [10], [11]. Substituting Eq. (16) in (15), the final compact equation for drain current becomes:

\[ I_d = 2W \mu_{\text{eff}} \frac{g_{\text{sat}}}{t_{\text{ox}}} \left( \frac{2kT q}{q} \right)^2 q_{\text{sd}} - q_{\text{sd}} + \frac{1}{2} \left( q_{\text{sd}}^2 - q_{\text{sd}} \right) \left( V_d - V_r \right) \]  

\[ + \frac{1}{2} \left( q_{\text{sd}}^2 - q_{\text{sd}} \right) \left( V_d - V_r \right). \]  

(17)

D. Quantum-Mechanical Effects (QMEs)

As the silicon fin width \( W_{\text{fin}} \) is scaled down to several nanometers (< 10 nm), quantum-mechanical effects become significant. To model QMEs, first we insert the carrier-energy quantization caused by the structural confinement, as a correction in the classical semiconductor work function. This correction results in an increase of the threshold voltage \( V_t \) by an amount given by [12], [13]:

\[ \Delta V_{\text{QME}} = \frac{(\pi \hbar)^2 \nu_{\text{sat}}}{2q_{\text{ox}} W_{\text{fin}}^2}. \]  

(18)

where \( \hbar \) is the reduced Planck’s constant and \( m_{\text{eff}} \) is the effective mass of electrons. A second effect arises from the quantum-mechanical distribution of the inversion charge, showing a peak inside the substrate at some distance away from the SiO2-Si interface [14]. This effect can be accounted for by considering two capacitances connected in series: the oxide capacitance formed by the physical oxide layer and the capacitance developed within the average distance of \( \Delta z \) inside the silicon from the interface [12], [13]. Thus, this quantum-mechanical effect results in an enhanced value of the gate oxide thickness given by:

\[ t_{\text{ox}} = t_{\text{ox}} + \Delta \Delta z. \]  

(19)

It was found that \( \Delta z \) has a constant value of about 1.2 nm derived from the difference of the average inversion layer depths [12]. The modified value of the oxide thickness causes...
shift of the threshold voltage by $\Delta V_{th,OM}$ calculated by replacing $t_{ox}$ with $t_{OM}^{OM}$. Thus, including the QMEs, the threshold voltage becomes:

$$V_{th}^{OM} = V_i + \Delta V_{th}^{OM} + \Delta V_{th,OM}. \tag{20}$$

By replacing $V_i$ with $V_i^{OM}$ and $t_{ox}$ with $t_{OM}^{OM}$, the drain current equation is rewritten as:

$$I_{d,OM} = 2W \mu_{eff,OM} \frac{E_s}{t_{ox}} \left[ \frac{2kT}{q} \right]^{\frac{1}{2}} \left[ \frac{q_{d,OM} - q_{d,OM}^{sat}}{L} \right] \left( 1 - \frac{q_{d,OM}^{sat} - q_{d,OM}^{sat}}{L - \Delta L_{OM}} \right). \tag{21}$$

Eq. (21) is a general unified equation for the drain current in TG FinFETs, which involves the secondary effects of SCEs, CLM, mobility degradation, series resistance and QMEs.

### III. Model Validation with Simulation Results

We have considered the device parameters: fin width $W_{fin} = 10$ nm, channel length $L = 20$ and 50 nm, fin height $H_{fin} = 40$ nm, equivalent gate oxide thickness $t_{ox} = 1$ nm, doping concentration of the silicon channel $N_A = 1.45 \times 10^{12}$ cm$^{-2}$, doping concentration of the source/drain contact regions $N_D = 10^{20}$ cm$^{-2}$ and midgap metal gate with work-function $4.71$ eV, constant electron mobility ($\mu_e = 200$ cm$^2$/Vs) and constant saturation velocity ($v_{sat} = 10^7$ cm/s).

We compared the drain current computed with the model and the device simulator for TG FinFETs. Figs. 2(a) and 3(a) show the transfer characteristics for drain voltages $V_D = 0.1$ and 1 V and the output characteristics for different $V_D$ values, respectively, for a short-channel ($L = 20$ nm) TG FinFET. The model current-voltage characteristics were derived using the parameters: $V_{th} = 0.1$ V, $v_{sat} = 1 \times 10^7$ cm/s, $\theta = 0.002$ and $R_{SD} W_{fin} = 1.2 \times 10^4$ Ohm cm and $c_1 = 2.65$. It can be seen that the model describes very well the current-voltage characteristics in all regions of operation. Figs. 2(b) and 3(b) show good agreement comparing the model with the simulation values of $g_{m}$ for different values of drain voltage and $g_{ds}$ for different values of gate voltage respectively.

The model has been validated also in devices with thin silicon layers, where the QMEs are significant. For QMEs, in Atlas 3D simulations, the “BQP” model was used with isotropic effective mass $m_e = 0.7x_m$, where $m_e$ is the free electron mass. In Fig. 4 the $I_D-V_D$ and $I_P-V_D$ characteristics calculated from the compact model for TG FinFET with parameters: $W_{fin} = 5$ nm, $L = 30$ nm, $H_{fin} = 30$ nm and $t_{ox} = 1$ nm, are compared with simulations using the model parameters of $\Delta z = 0.6$ nm and $V_{th}^{OM} = 0.005$ V. It is evident the good agreement between model and simulated results.

### IV. Conclusion

An analytical and compact drain current-voltage model for undoped (or lightly doped) short-channel triple-gate (TG) FinFETs, accounting for small-geometry effects and quantum mechanical effects, is presented. The model is an extension of the compact model for double-gate (DG) FinFETs with increasing the channel width by the top-gate width and incorporating the effect of the top-gate on the short-channel effects through the threshold voltage modeling. The proposed model has been validated by device simulations in all regions of operation for channel lengths down to 20 nm.

### Acknowledgment

We would like to thank the Greek Ministry of Education, Long Life Learning and Religious Affairs, General Secretariat for Research and Technology for financial support under the Program COOPERATION with contract number 09-SYN-42-998.

### References


