Analog/RF Performance: Are SOI FinFETs better than DG SOI MOSFETs?

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Abstract—Analog/RF performance of nanoscale triple gate FinFETs and planar single gate and double gate SOI MOSFETs is examined via extensive 3D device simulations. Well-designed DG MOSFETs attain higher values of cut-off frequency for both lower and higher drain currents, whereas FinFETs offer higher intrinsic gain while compromising cut-off frequency. For longer channel lengths, SG MOSFETs show slightly higher cut-off frequency in comparison to multi-gate (MG) MOSFETs, whereas MG MOSFETs exhibit higher cut-off frequency for lower channel lengths. A unique figure of merit, gain transconductance frequency product (GTFP) for best trade-off among gain, transconductance, and speed is compared. DG MOSFETs exhibit higher GTFP over a wide range of device scaling, thus remain a good candidate for analog/RF applications. Furthermore, the RF linearity performance of these devices has been examined.

Index Terms— DG MOSFETs, FinFETs, Analog/RF performance, linearity, ATLAS device simulator

I. INTRODUCTION

FinFET is an emerging CMOS device that uses a novel architecture allowing the control of short-channel effects by means of the 3D geometry [1]. Technologically, FinFETs can be fabricated as a triple gate (TG) or as a double gate (DG) device [2]. FinFETs are mainly fabricated on SOI substrates [3]; bulk FinFETs have also gained attention due to their low-cost process and their compatibility with standard bulk CMOS technology. Structurally, bulk FinFETs and SOI FinFETs are similar, except for the fact that bulk FinFETs use an isolation oxide layer (SiO₂) between the bottom gate electrode and the bulk Si surface to avoid gate electrode contacting the Si wafer [4]. Bulk FinFETs with junction depths corresponding to the bottom of the gate have higher subthreshold slope and drain induced barrier lowering (DIBL) in comparison with SOI FinFETs [5]. Double gate (DG) SOI MOSFETs are also well suited for ultra-low-voltage operation due to the inherent suppression of short channel effects (SCEs), excellent scalability and reduced DIBL [6]-[8]. Recently, the impact of various design engineering approaches, which are easily adaptable to DG MOSFETs and can improve analog/RF performance, are reported by Sharma et al., [9], [10]. The crucial issue of gate misalignment associated with nanoscale planar DG MOSFETs can effectively be reduced by graded channel architecture [11], [12].

A comparison of nanoscale MOS device architectures for analog/RF performance has been undertaken by a number of scientific groups [13]-[15]. The cut-off frequency \( f_T \) for SG MOSFETs is comparable to MG MOSFETs, whereas intrinsic gain for SG devices is extremely low. DG MOSFETs show higher \( f_T \), whereas FinFETs offer better intrinsic gain while compromising \( f_T \). It is therefore very difficult to decide which device performs better than the other in terms of overall analog/RF performance. In this article, a close comparison between single-gate (SG), symmetric DG SOI MOSFETs and triple gate (TG) SOI FinFETs is done by means of a unique figure of merit, gain transconductance frequency product (GTFP). GTFP comprises, beyond the transconductance efficiency and the switching speed, also the information on intrinsic gain [10]. The peak of GTFP occurs in the moderate inversion, an interesting region for circuit designers. A comparison of GTFP among DG and FinFETs is done for channel lengths down to 15 nm while for SG MOSFETs, analysis is limited to 22 nm channel length, due to adverse short channel effects (SCEs). The important analog/RF figures of merit like

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transconductance-to-drain current ratio \((g_m/|I_{DS}|)\), intrinsic gain \((g_m/g_d)\), total capacitances \((C_{ss})\), cut-off frequency \((f_t)\) and maximum frequency of oscillation \((f_{max})\) are examined. Furthermore, device linearity is an important figure of merit in RFIC design which ensures that intermodulation and high-order harmonics are minimal at the output [16], [17]. Hence the linearity performance of these devices has also been investigated.

II. DEVICE STRUCTURES

Schematic diagrams of simulated symmetric DG MOSFET and of the TG FinFET are shown in Fig. 1. Since the drain current flows on the top and on the sidewalls of the fin, the total effective width for FinFET is computed as \(W = (2H_{FIN} + W_{FIN})\), with \(H_{FIN} = 30\) nm [18]. 3D simulations of SG and DG SOI MOSFETs have been carried out with the same width \(W_{SG} = 2W_{DG} = 2(H_{FIN} + W_{FIN})\) as that of FinFETs. The equivalent gate oxide thickness (EOT) of 1.1 nm, silicon film thickness \(T_{si}\) of 8 nm, silicon film doping of \(1 \times 10^{15}\) cm\(^{-3}\) has been chosen to minimize short channel effects and comply with ITRS requirements. The high doping concentration of \(1 \times 10^{20}\) cm\(^{-3}\) for source/drain, metal gate work-function \((\Phi_M)\) of 4.46 eV and buried oxide thicknesses \(T_{BOX}\) of 25 nm is used in the simulations unless stated otherwise.

Fig. 1. The schematic structures of n-channel (a) FinFET (b) DG SOI MOSFET.

III. TCAD CALIBRATION

TCAD is a very powerful tool to simulate nanoscale transistors, however it needs to be calibrated for simulation of FinFET as current flow in actual FinFETs is dominated by <110> plane. Calibration of the TCAD tool has been done by matching dc characteristics of fabricated FinFETs data (Intel) with that of the simulated devices as shown in Fig. 2. It is observed that drift-diffusion models with default parameters underestimate the ON current as compared to experimental data. However, hydrodynamic models with default parameters overestimate the ON current. Calibrated hydrodynamic models along with Lombardi CVT mobility model with calibrated parameters have been used. The matching has been mainly achieved by tuning the mobility values. Significant quantum confinement of the carriers is expected because of the small fin width; Bohm quantum potential model with calibrated parameters has been used to account for this phenomenon. Shockley–Read–Hall recombination/generation with doping-dependent carrier lifetime and Auger recombination along with Fermi-Dirac statistics have been taken into consideration. The calibrated model parameters are used for all the TCAD simulations reported in this paper.

IV. RESULTS AND DISCUSSION

In Fig. 3, transconductance \((g_m)\) of SG, DG and FinFET is compared in saturation while maintaining the same off current \((I_{OFF} \sim 2.0\) nA) for DG and FinFET. It is difficult to match \(I_{OFF}\) of SG devices to DG and FinFET, so for a fair comparison, \(V_{th}\) of SG made equivalent to DG and FinFETs by adjusting the gate workfunction and channel doping. The \(V_{th}\) is defined as the gate bias when the drain current reaches \(1 \times 10^{-6}\) A and found to be 0.216 V at \(V_{DS} = 1.0\) V. SG devices show lower \(g_m\) values due to significant SCEs. FinFET devices demonstrate the same \(g_m\) when
compared with DG MOSFETs at lower gate voltage, however improved $g_m$ at higher gate voltage due to better gate control (top gate) over the channel region.

The $g_m/\text{I}_{DS}$ ratio demonstrates how efficiently the current is used to achieve a certain value of transconductance. The advantage of high transconductance-to-drain current ratio is the realization of circuits operating at low supply voltage. As shown in Fig. 4, the $g_m/\text{I}_{DS}$ ratio is maximized in the subthreshold region of device operation. In this region, the $g_m/\text{I}_{DS}$ ratio for both DG and FinFETs is almost similar, however $g_m/\text{I}_{DS}$ for FinFETs is slightly improved at higher levels of drain current due to better SCEs. SG MOSFETs exhibit much lower $g_m/\text{I}_{DS}$ due to drastically higher off current.

The FinFET devices provide a better gain when compared with DG as shown in Fig. 5. The improved performance of FinFET design is because of excellent gate control over the channel region that results in higher transconductance and reduced output conductance. SG devices show much lower intrinsic gain due to large short channel effects which result in higher output conductance ($g_{ds}$) in saturation along with lower $g_m$.

![Fig. 3. Variation of transconductance ($g_m$) with gate voltage ($V_{GS}$) for a fixed drain voltage of $V_{DS} = 1.0\, \text{V}$.](image)

![Fig. 4. Transconductance efficiency as a function of drain current ($\text{I}_{DS}$) for a drain voltage of $V_{DS} = 1.0\, \text{V}$.](image)

![Fig. 6. Dependence of total gate capacitance ($C_{gg}$) on gate voltage for a drain voltage of $V_{DS} = 1.0\, \text{V}$.](image)
difficult to minimize and thus limits the RF performance. The capacitance for SG devices is quite similar to that of DG devices.

![Graph showing f_T and f_max vs. I_Ds for SG MOS, DG MOS, and FinFET.](image)

Fig. 7. The variation of cut-off frequency (f_T) and maximum frequency of oscillation with drain current (I_Ds) at V_DS = 1.0 V.

Cutoff frequency (f_T) and maximum oscillation frequency (f_max) are two important parameters for evaluating the RF performance of the device. Generally, f_T is the frequency when the current gain is unity, whereas f_max is the frequency at unity power gain. In the present analysis, f_T and f_max are calculated as follows:

\[
f_T = f_0 \left| H_{21} \right| H_{21} = \frac{Y_{21}}{Y_{11}}
\]

\[
f_{\text{max}} = f_0 \sqrt{\frac{\left| Y_{21} - Y_{12} \right|^2}{4 \left[ \text{Re}(Y_{11}) \text{Re}(Y_{22}) - \text{Re}(Y_{12}) \text{Re}(Y_{21}) \right]}}
\]

DG SOI MOSFETs demonstrate higher f_T and f_max in comparison to SG MOSFETs and FinFETs as shown in Fig. 7, thus a good candidate for high speed switching applications. Note that at high values of drain currents, planar SG SOI MOSFETs achieve nearly the same f_T as of FinFET.

The product of g_m/I_Ds and f_T represents a trade-off between power and bandwidth and is utilized in moderate-to-high speed designs [20], [21]. Fig. 8 shows the variation of transconductance frequency product (TFP = g_m/I_Ds x f_T) with drain current. Note that DG offers much higher TFP when compared with FinFETs and SG device. The lower value of TFP for SG devices is due to worse g_m/I_Ds ratio degraded due to strong DIBL. It is important to note that peak of TFP for SG devices occurs at the higher end of moderate inversion (closer to the onset of strong inversion) when compared with DG and FinFETs.

![Graph showing TFP vs. I_Ds for SG MOS, DG MOS, and FinFET.](image)

Fig. 8. Transconductance frequency product (TFP) as a function of the drain current (I_Ds) for V_DS = 1.0 V.

DG MOSFETs show higher f_T while FinFETs offer better intrinsic gain. It is very difficult to decide which device performs better than the other in terms of overall performance. Thus, a unique figure of merit, gain transconductance frequency product (GTFP = g_m/I_Ds x g_m/I_Ds x f_T) is used as an additional means of comparing the overall performance of SG, DG and FinFET devices. The variation of GTFP with drain current is shown in Fig. 9. It is quite clear that DG MOSFETs exhibit higher GTFP when compared to FinFETs. This is due to superseding of higher f_T of DG MOSFETs over the better intrinsic gain of FinFETs. Note that the peak value of GTFP occurs at a quite low level of drain current, in the vicinity of I_Ds = 8.2 µA, corresponding to the transition from moderate to strong inversion (V_GS = 0.3 V). This provides valuable information for circuit designers, allowing them to determine the optimal region achieving the best overall trade-off among gain,
transconductance, and speed. As expected, SG devices show much lower GTFP and peak of GTFP occurs at slightly higher $I_{DS}$ in comparison to MG devices.

The variation of peak value of $f_T$ and $f_{max}$ for SG, DG and FinFETs with channel length ($L$) is shown in Fig. 10. All the devices have been compared at similar $V_{th}$ for each length. The simulated $f_T$ and $f_{max}$ for SG devices have been verified with the measured data [22]-[24] and ITRS predictions [25], as shown in the same figure. Note that SG devices offer marginally better $f_T$ for longer channel lengths. As expected, FinFETs demonstrate lower $f_T$ due to higher capacitance. For shorter channel lengths, DG MOSFETs offer higher $f_T$ and $f_{max}$ when compared with other devices. The results for $f_T$ and $f_{max}$ are in close proximity to measured data and ITRS predictions and thus validate our ac simulations.

The peak values of analog/RF figures of merit like transconducance-to-drain-current ratio ($g_m/I_{DS}$), intrinsic gain ($g_m/g_{ds}$), cut-off frequency ($f_T$), transconductance frequency product (TFP = $g_m/I_{DS} \times f_T$) and gain transconductance frequency product (GTFP = $g_m/g_{ds} \times g_m/I_{DS} \times f_T$) are compared for SG, DG and FinFET devices in Table 1. Physical parameters chosen for $L = 15$ nm simulation are different from 22 nm, to minimize SCEs. However, for $L = 32$ nm and 45 nm simulation, similar physical parameters are taken to that of 22 nm. Note that the peak values of TFP and GTFP for MG devices correspond to $V_{GS}$ just about 80 mV above the threshold voltage of the device. This is valuable information for circuit designers, allowing them to determine the optimal region achieving the best overall trade-off among gain, transconductance, and speed. The peak of intrinsic gain
shifts towards higher $V_{GS}$ with device scaling. It is quite clear that DG MOSFETs outperform other devices in terms of overall analog/RF performance up to very short gate length.

### Table1

Peak values of analog/RF figures of merit and corresponding $V_{GS}$

<table>
<thead>
<tr>
<th>Devices</th>
<th>$g_{m,dr} (V^2)$</th>
<th>$g_{dr} / g_{m}$</th>
<th>$f_t (GHz)$</th>
<th>$TFP (×10^6)$</th>
<th>$GTFP (×10^6)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>DG</td>
<td>29.0</td>
<td>33.5 (0.65)</td>
<td>701 (0.70)</td>
<td>7.68 (0.20)</td>
<td>1.88 (0.20)</td>
</tr>
<tr>
<td>FinFET</td>
<td>28.9</td>
<td>36.9 (0.65)</td>
<td>640 (0.65)</td>
<td>5.97 (0.20)</td>
<td>1.71 (0.20)</td>
</tr>
<tr>
<td>SG</td>
<td>19.6</td>
<td>7.94 (0.65)</td>
<td>391 (0.65)</td>
<td>3.52 (0.30)</td>
<td>0.26 (0.30)</td>
</tr>
<tr>
<td>DG</td>
<td>32.3</td>
<td>44.1 (0.60)</td>
<td>448 (0.65)</td>
<td>5.91 (0.30)</td>
<td>2.01 (0.30)</td>
</tr>
<tr>
<td>FinFET</td>
<td>32.2</td>
<td>51.4 (0.60)</td>
<td>396 (0.60)</td>
<td>5.09 (0.30)</td>
<td>1.83 (0.30)</td>
</tr>
<tr>
<td>SG</td>
<td>26.4</td>
<td>21.6 (0.40)</td>
<td>290 (0.60)</td>
<td>2.95 (0.30)</td>
<td>0.46 (0.30)</td>
</tr>
<tr>
<td>DG</td>
<td>36.6</td>
<td>121 (0.35)</td>
<td>311 (0.60)</td>
<td>5.34 (0.325)</td>
<td>6.40 (0.325)</td>
</tr>
<tr>
<td>FinFET</td>
<td>36.6</td>
<td>140 (0.35)</td>
<td>278 (0.60)</td>
<td>4.68 (0.325)</td>
<td>6.02 (0.325)</td>
</tr>
<tr>
<td>DG</td>
<td>33.0</td>
<td>46.1 (0.35)</td>
<td>230 (0.60)</td>
<td>3.23 (0.30)</td>
<td>1.45 (0.30)</td>
</tr>
<tr>
<td>FinFET</td>
<td>38.1</td>
<td>302 (0.25)</td>
<td>225 (0.60)</td>
<td>4.34 (0.325)</td>
<td>12.0 (0.325)</td>
</tr>
<tr>
<td>FinFET</td>
<td>37.9</td>
<td>324 (0.25)</td>
<td>202 (0.60)</td>
<td>3.65 (0.325)</td>
<td>11.0 (0.325)</td>
</tr>
</tbody>
</table>

Linearity is an essential requirement in all RF systems, ensuring that inter-modulation and high-order harmonics are minimal at the output [26]. The third-order nonlinearity term, $g_{m3}$, is especially troublesome for RF systems, since it leads to inter-modulation, i.e. distortion of the fundamental amplitude via signals in the adjacent bands. In fact, radio distortion is mainly determined by the 3rd order derivative of the drain current to the gate voltage i.e. VIP3. For low distortion, a large VIP3 is required.

$$\text{VIP3} = \sqrt{\frac{24 g_m}{g_{m3}}}$$

where $g_m$ is the transconductance and $g_{m3}$ is the 3rd-order derivative of the drain current versus gate bias and VIP3 is the extrapolated input voltage amplitude at which the first and the 3rd order output amplitude are equal. Fig. 12 shows the variation of VIP3 with drain current at $V_{DS} = 1.0$ V. DG MOSFETs show peak VIP3 (less distortion) in comparison to other devices. SG devices offer slightly better linearity performance than MG FETs. Of particular interest is the local peak corresponding to the so-called “sweet spot”, favored by RF designers. Note that the latter occurs at moderate levels of current, that incidentally are located within the same range of current where TFP (Fig. 8) and GTFP (Fig. 9) present their peaks.

Furthermore, a reliable and simple metric used to evaluate linearity performance of individual RF devices is the third-order intercept point (IP3). This measures the input power (PIP3) where the 3rd-order inter-modulation term ($2\alpha_2 - \alpha_1$) at the output is equal to the main harmonic ($\alpha_1$). For an amplifier, assuming a matched input resistance $R_s = 50 \Omega$, PIP3 can be expressed in terms of nonlinearity coefficients [26].

$$\text{PIP3} = \frac{2g_m}{3g_{m3}R_s}$$

The output conductance can also introduce nonlinearities. However, for relatively low values (50Ω) of the input resistance, the influence of the output conductance is minimal [27]. The variation of PIP3 with drain current at $V_{DS} = 1.0$ V is shown in Fig. 13. Similar to VIP3, DG MOSFETs show slightly improved PIP3 in comparison to FinFETs.
V. CONCLUSION

Analog/RF performance of nanoscale SG, DG SOI MOSFETs and TG SOI FinFETs is compared by means of TCAD device simulations. Analog/RF figures of merit, ranging from transconductance efficiency and cut-off frequency to intrinsic gain and linearity, have been analyzed concurrently. The two figures of merit, transconductance frequency product (TFP) and gain transconductance frequency product (GTFP) show a distinctive peaking at moderate levels of current. SG devices exhibit comparable \( f_T \) and TFP for longer channel length but much lower TFP and GTFP for shorter channel length, compared to MG devices. The peak of TFP and GTFP for SG devices occurs at the higher end of moderate inversion. TFP follows the cut-off frequency behavior whereas GTFP is governed by intrinsic gain of the device. With decreasing channel length, the enhancement in TFP for DG devices becomes more significant, while an almost uniform decrease in GTFP is observed. DG MOSFETs offer peak \( f_T \) and \( f_{max} \) along with much better TFP when compared to SG MOSFETs and TG FinFETs. DG MOSFETs also demonstrate higher GTFP down to very short channel length and show quite good linearity performance, and thus remain a good candidate for analog/RF applications. Finally, the ‘sweet spot’ of high linearity performance has been shown to be closely related to the occurrence of the peak TFP and GTFP regions. Hence, the region of best analog/RF performance including high linearity can be found at very moderate levels of current, for gate voltage in close vicinity around threshold.

REFERENCES


